SGS-THOMSON MICROELECTRONICS

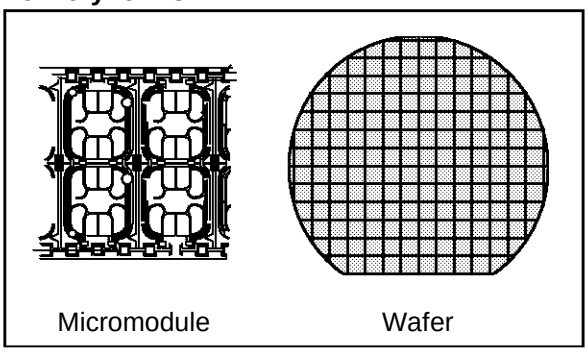
ST1331, ST1333 ST1335, ST1336

HIGH ENDURANCE CMOS 272 Bit EEPROM WITH SECURE LOGIC ACCESS CONTROL

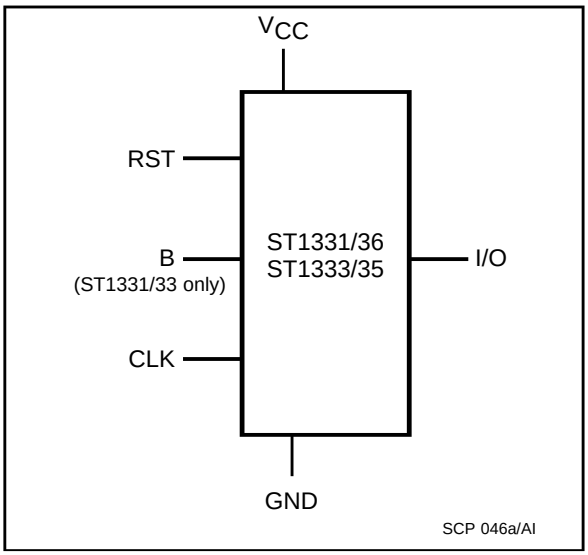
BRIEF DATA

- SINGLE 5 VOLTS POWER SUPPLY
- HIGHLY RELIABLE CMOS EEPROM TECHNOLOGY:
  - 10 years data retention
  - 1 Million Erase/Write cycles endurance
- PROGRAMMING TIME < 5 MS.
- MAIN MEMORY DIVIDED INTO :
  - 16 bits of chip identification data
  - 48 bits of card identification data
  - 40 bits of counter
  - 16 bits for validation certificate
  - 64 bits for authentication secret key (ST1333/35) / issuer defined area (ST1331/36)
  - 32 bits for anti-tearing flags (disconnected by option)
  - 56 bits of user defined data (not erasable by option)
- COUNTER CAPACITY UP TO 32767 (8^5 -1) UNITS.
- CERTIFICATE FOR CARD VALIDATION
- ADVANCED AUTHENTICATION FUNCTION (ST1333/35)
- 24 BITS TRANSPORT CODE.
- SPECIAL ANTI-TEARING MECHANISM.
- RESET ON VCC HIGH AND LOW.
- TWO COMMUNICATION PROTOCOLS POSSIBLE:
  - 6 contacts for ST1331/33
  - 5 contacts for ST1335/36
- E.S.D. > 4000 VOLTS.

Delivery forms



Pin Connection



ST133x family Products

Product	Advanced Authentication function	Communication Protocol	
		6 contacts	5 contacts
ST1331		Yes	
ST1333	Yes	Yes	
ST1335	Yes		Yes
ST1336			Yes

Contact name

CLK	Clock
RST	Function code for ST1331/33
	Reset for ST1335/36
B	Function Code for ST1331/33
I/O	Data Input / Output
Vcc	Supply Voltage
GND	Ground

DESCRIPTION

The ST133x circuits, mainly dedicated to prepaid phone card applications, are a 272 bit EEPROM protected by hardwired security logic and special "fuses". The memory is a matrix of 34 x 8 cells accessed bit by bit for reading and programming and by byte for internal erasing. An on-chip address counter provides an internal adressing space up to 512 bits.

These circuits include an identification data area, basic units counter with an anti-tearing counting mechanism (for proper usage in open readers), a post validation certificate, an issuer defined area (ST1331/36) or a special authentication secret key (ST1333/35), and user defined area.The validation certificate implemented in the memory allows the recognition of the circuit by the appropriate security module.

The anti-tearing mechanism allows the prevention of any loss of units in the case of an aborted operation when using an open reader (unwanted extraction).

This circuit receives 4 commands through external pads: RESET, which resets address to 000d, READ which increments address and reads the corresponding data and, COMPARE which allows internal transport code comparison with presented code, finally PROGRAM which changes the memory contents. Two communication protocols are possible: ST1335/36 use 5 contacts (Vcc, GND, I/O, CLK and RST) while ST1331/33 also use an additional contact (B).

The circuits can be used in 2 different CONFIGURATIONS in NORMAL mode: the first one is for the ISSUER (Card manufacturer) where special data can be written into the chip during initialisation and the second one is for the final USER.

Two options can be chosen on ordering :

– The anti-tearing mechanism can be disconnected. In this case, the anti-tearing flag area from bit 288d to bit 319d is unused (seeFigure 3, Memory Mapping, on page 3).
– The user defined area from bit 320d to bit 375d can be defined as "not erasable" in USER configuration.

EXTERNAL COMMANDS

SIX CONTACT COMMUNICATION PROTOCOL

This set of commands is defined to be fully compatible with existing FRANCE TELECOM system.

The 4 commands are defined by sampling the state of RST and B lines on the rising edge of CLK as indicated in the table below.

RST	B	CLK	COMMAND
0	0	0 --> 1	RESET & READ 000d
1	0	0 --> 1	NO EFFECT
0	1	0 --> 1	INCREMENT ADDRESS & READ DATA
0	1	0 --> 1 1 --> 0	INCREMENT ADDRESS & COMPARE
1	1	0 --> 1	PROGRAM

The circuit is connected to an external resistor on I/O line. For this protocol a PROGRAMMED bit is read as a logic "1" (I/O line = Vcc), an ERASED bit is read as a logic "0" (I/O line = Gnd).

FIVE CONTACT COMMUNICATION PROTOCOL

This set of commands is defined to be fully compatible with existing ST1305 circuits or like.

The RESET and READ commands are defined by sampling the state of RST line on the rising edge of CLK, while the PROGRAM command is selected by a high level pulse on RST line before a CLK pulse as indicated in the table below.

RST	CLK	COMMAND
1	0 --> 1	RESET & READ 000d
0	0 --> 1	INCREMENT ADDRESS & READ DATA
0	0 --> 1 1 --> 0	INCREMENT ADDRESS & COMPARE
0 -> 1 -> 0 0	0 0 --> 1	PROGRAM

The circuit is connected to an external resistor on I/O line. For this protocol a PROGRAMMED bit is read as a logic "0" (I/O line = GND), an ERASED bit is read as a logic "1" (I/O line = Vcc).

Memory Mapping